Notice of Allowability	Application No.	Applicant(s)	
	10/712,971	NAKATANI ET AL.	
	Examiner	Art Unit	
	Quochien B. Vuong	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/13/2003*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Reasons for Allowance

1. Claims 1-25 are allowed over the cited prior art.

2. The following is an examiner's statement of reasons for allowance:

Regarding independent claims 1 and 14, Akiyama (US 6,037,634) disclose a semiconductor differential circuit and method (figures 1 and 2) comprising: a semiconductor substrate (1), a first semiconductor device (PMOS) and a second semiconductor device (NMOS) formed on said semiconductor substrate having drain electrode and gate electrode (column 7, lines 14-58); and Funaika et al. (US 6,211,549) disclose semiconductor differential circuit and method (figures 2 and 3A-3C) comprising: a semiconductor substrate, a first semiconductor device and a second semiconductor device formed on said semiconductor substrate having drain electrode and gate electrode (column 2, line 23- column 3, line 26; and column 6, line 6 – column 7, line 42). However, Akiyama and Funaika, either alone or in combination, fail to further disclose the semiconductor differential circuit and method wherein the first semiconductor having a first gate electrode for having one of differential signals conveyed thereto and a first drain electrode for outputting one of the differential signals controlled by the first gate electrode; the second semiconductor device having a second gate electrode for having the other of the differential signals conveyed thereto and a second drain electrode for outputting the other of the differential signals controlled by the second gate electrode, and wherein the first drain electrode and the second drain electrode are placed in a proximity so that, at a predetermined frequency, it is equivalent to the one in which the first drain electrode is grounded via a first

predetermined resistance, and the second drain electrode is grounded via a resistance of the same resistance value as the first predetermined resistance.

Regarding independent claim 10, Akiyama (US 6,037,634) disclose a semiconductor differential circuit and method (figures 1 and 2) comprising: a semiconductor substrate (1), a first semiconductor device (PMOS) and a second semiconductor device (NMOS) formed on said semiconductor substrate having collector or base (column 7, lines 14-58); and Funaika et al. (US 6,211,549) disclose semiconductor differential circuit and method (figures 2 and 3A-3C) comprising: a semiconductor substrate, a first semiconductor device and a second semiconductor device formed on said semiconductor substrate having collector or base (column 2, line 23- column 3, line 26; and column 6, line 6 – column 7, line 42). However, Akiyama and Funaika, either alone or in combination, fail to further disclose the semiconductor differential circuit wherein the first semiconductor having a first collector or base for having one of differential signals conveyed thereto; and a second semiconductor device having a second collector or base for having the other of the differential signals conveyed thereto, and wherein: the first collector or base and the second collector or base are placed in a proximity so that, at a predetermined frequency, it is equivalent to the one in which the first collector or base is grounded via a second predetermined resistance, and the second collector or base is grounded via a resistance of the same resistance value as the second predetermined resistance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakakura (US 4,695,479) discloses MOSFET semiconductor device and manufacturing method thereof.

Ohmi (US 5,021,843) discloses semiconductor integrated circuit.

Omura et al. (Us 6,037,632) disclose semiconductor device.

Sakamoto (US 6,316,296) discloses field-effect transistor and method of manufacturing same.

Yamaguchi et al. (US 6,650,001) disclose lateral semiconductor device and vertical semiconductor device.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B. Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quochien B. Vuong
Mar. 19, 2006.

QUOCHIEN B. VUONG
PRIMARY EXAMINER